**Processor Manual**

This circuit supports the following operations :

**OPERATION**  **OPCODE**

MOV 000 000

MOV IMMEDIATE 100 001

ADD 000 010

ADD IMMEDIATE 100 011

SUB 000 100

SUB IMMEDIATE 100 101

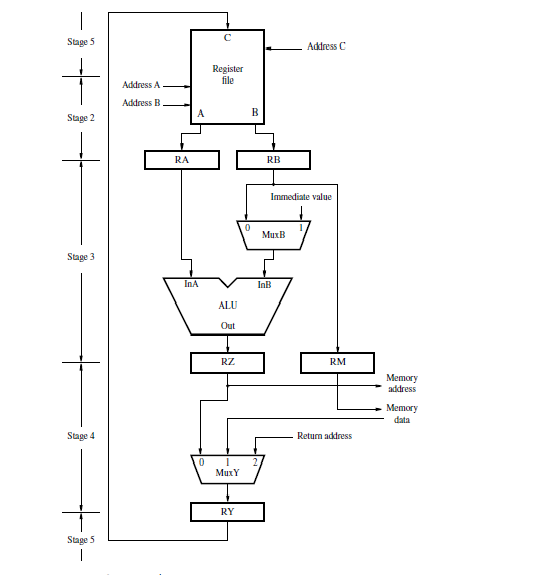
LOAD 000 110

STORE 000 111

If most significant bit is 1, it will indicate that an immediate value is present. Thus a control signal will be generated which will enable input 1 of MUXB.

Similarly a control signals for MUXY is generated which will enable 1 in case of load.

Two control Signals are generated from Control Unit for memory operations (Load and Store).



**How to Perform Operations:**

**MOV :**

**MOV R1, R2**

**R1 = Address 1 (5 bit input).**

**R2 = Address 2 (5 bit input).**

This command will perform this operation **[R1] <- [R2].**

**MVI:**

**MVI R1, value**

**R1 = Address 1 (5 bit input).**

**Value = 16 bit input value.**

This command will perform this operation **[R1] <- value.**

**ADD:**

**ADD R1, R2**

**R1 = Address 1 (5 bit input).**

**R2 = Address 2 (5 bit input).**

This command will perform this operation **[R1] <- [R1] + [R2].**

**ADD IMMEDIATE:**

**ADI R1, value**

**R1 = Address 1 (5 bit input).**

**Value = 16 bit input value.**

This command will perform this operation **[R1] <- [R1] + value.**

**SUB:**

**ADD R1, R2**

**R1 = Address 1 (5 bit input).**

**R2 = Address 2 (5 bit input).**

This command will perform this operation **[R1] <- [R1] - [R2].**

**SUB IMMEDIATE:**

**ADI R1, value**

**R1 = Address 1 (5 bit input).**

**Value = 16 bit input value.**

This command will perform this operation **[R1] <- [R1] - value.**

**LOAD:**

**LOAD R1,R2**

**R1 = Address of memory whose data is to be fetched(5 bit input).**

**R2 = Register in which fetched data is to be stored (5 bit input).**

**STORE:**

**STORE R1,R2**

**R1 = Address of memory where data is to be stored (5 bit input).**

**R2 = Register which contains data to be stored (5 bit input).**

In my circuit , module named RegisterFile is driving module.

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